REMARKS

In response to the claim rejection under 35 U.S.C. 112, on page 2 of the Office Action, the applicant explains Examiner's queries as follows:

As to whether an initializing process is required prior to effect accessing commands, it is noted that initial values are written in the memories as given initial values. However, these initial values are not required to be set to all "zeros" or "ones." In other words, "One" or "zero" may be optionally set in the memory cell as a given initial value.

Based on the description on page 6, line 4, accessing commands in claim 1 includes any writing, reading or refreshing operations.

According to the description quoted from page 5 lines 6-13, *"The method in accordance with the present invention is composed of at least two steps: the main step and the data checking step. In the main step, ...**Afterwards, the data checking step provides checking commands that check addresses yet to be triggered in the main step, i.e., the even columns (rows).**"*, checking commands check the memory addresses yet to be triggered in the main step.

For one skilled in the memory testing field, "checking command" represents reading the present memory values, and then comparing the present memory values with the given initial values.

As mentioned in the description of page 5, while command actions are applied to the odd columns, the yet to be accessed memory addresses, i.e. the even columns, weakened memory addresses in the even columns may possibly be induced by the electromagnetic interference (EMI) because of the command actions. Afterwards, when the data checking step provides checking commands to check the even columns addresses, the weakened memory is thus detected.

With regard to claims 4-6, the applicant incorporates claims 5 and 6 into claim 4. In the present amended claim 4, the subject matter sought to be patented is a memory test method in which

a step of executing a test program is involved, where the test program is further recited to include command actions as well as checking actions. The applicant asserts that claim 4 is indeed a process as required by 35 U.S.C. 101, because claim 4 is neither a mathematical formula nor an algorithm.

In response to the applicant's previous argument of December 11, 2003, the Examiner still maintains that claims 1-6 and 11-13 are unpatentable over the prior art of record.

With reference to the prior art disclosed by the applicant himself (hereinafter admitted prior art), the conventional memory testing method uses accessing commands (read, write or refresh commands) to test all memory cells **one bit by one bit**. For example, as shown in Fig. 6A, when accessing the first row from left to right, the EMI may result in weakening the next row.

However, after finishing the access of the first row and starting the access of the subsequent row, the second row is strengthened from the weakened state to a normal state due to the accessing commands applied on the second row. Therefore, the weakened memory is unable to be detected.

However, the present claims 1-6 and 11-13 clearly recite that the testing method indeed has two acts. For example, claim 1 reads:

"sequentially performing accessing commands on the **odd addresses** in the memory array;

and sequentially performing data checking commands on the **even addresses** in the memory array that are complementary to the odd addresses."

In the first step, the accessing commands are only applied to the odd addresses of the memory. That means only a half of memory cells are processed by read, write or refresh commands, no all memory cells. In the next step, the claim clearly recites that data checking commands are performed on the even addresses, i.e. the rest of the memory cells are not performed on by the accessing commands. In the aspect of the literal meanings represented in claim 1, said claim has explicitly distinguished the difference between the admitted prior art and the invention. Therefore,

the descriptions of the aforementioned two steps should be deemed as obvious limitations that are truly not disclosed in the admitted prior art.

With references to the cited US. Patent 4,513,374 (Hooks hereinafter), the Examiner indicated that since Hooks, as seen in col. 1 line 8 et seq., is related to memory systems for use in storing data for image processor, it is conceivable that the address generation approach thereof be of practical use in any memory systems, including test systems for such memory. Further, the Examiner also notes that to establish a prima facie case of obviousness, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art.

After reviewing the cited U.S. Patent 4,513,374, the applicant admits that Hooks indeed disclosed a memory system. However, the purpose of the memory system is for use in the image processing systems, not for use in the memory test. Based on the entire description of the patent, Hooks's disclosure obviously is directed to improve image generating process by his memory system. Even in col. 5 lines 19-24 of the patent, which is pointed out by the Examiner in the first Office Action to reject the referenced application under 35 U.S.C. 103(a), Hooks's disclosure is still directed to the image generating process. In column 20, line 21, the description is directed to produce interlaced video. Further, in line 23, which reads "...540 for even fields and ...540 for odd fields, it is noted that 540 is the number of pixel(s). The description in column 20, lines 44 further explicitly explains the image generating process, which reads

> *"However, when it is desired to monitor the signal on a monitor screen, it must be input into the monitor in the interlaced mode for clarity of viewing, and the signal stored in the non-interlaced mode in the frame*

buffer memory 214 is converted to interlaced mode by being read out in interlaced mode."

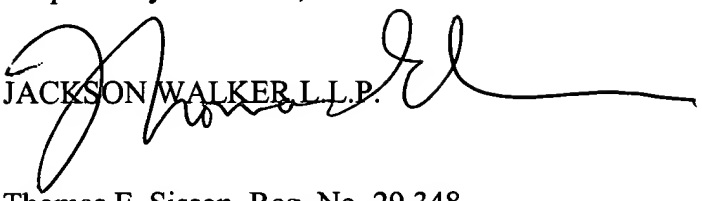
It is noted that what is interlaced is the way in which the image signal is input into the monitor, and Hooks does not mention any memory testing problems or approaches either in the background or the detailed description. Memory devices have been widely used in many electronic apparatus or systems. To fit a unique requirement, a particular memory system may be proposed, as such in Hooks's disclosure. However, such a memory system is not directed to a "memory testing" technique, and should not be deemed as conceivable for a person to base on the memory system to find a solution for overcoming problems of memory test.

For one skilled in the memory testing field, it is questionable whether there will be a motive to refer to this cited patent. Furthermore, a key point of concern is that the objective of the present invention is to detect the weakened memory cells. Therefore, even referring to Hooks's description, another question is whether the image interlacing process can inspire one to propose a solution for weakened memory detecting, as in the present invention.

Although the Examiner indicates that when establishing a prima facie case of obviousness, the knowledge generally available to one of ordinary skill in the art is a basis, the applicant asserts that the "one of ordinary skill in the art" should be interpreted as one of ordinary skill in the memory testing art, **not** in the image processing art.

The applicant, therefore, respectfully asks the Examiner to reconsider his basis for rejection of the claims and issue a Notice of Allowance.

Respectfully submitted,



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Date: 6-21-04

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